USN | | | | | | | | | | |

06EC74

Seventh Semester B.E. Degree Examination, December 2011

DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the two methods of sampling rate conversions used in DSP system, with suitable block diagrams and examples. Draw the corresponding spectrum. **(08 Marks)**

b. List the major architectural features used in DSP system to achieve high speed program execution. **(06 Marks)**

c. Explain how to simulate the impulse responses of FIR and IIR filters. **(06 Marks)**

2 a. With a neat block diagram, explain arithmetic logic unit (ALU) of DSP system. **(06 Marks)**

b. Explain the operation of barrel shifter, with an example. **(05 Marks)**

c. Explain : i) Circular addressing mode ii) Parallelism iii) Guard bits. **(09 Marks)**

3 a. Explain functional architecture of TMS320C54XX processor, with a block diagram. **(10 Marks)**

b. Explain the addressing modes of TMS320C54XX processor. Give examples. **(10 Marks)**

4 a. Describe the pipelining operation of TMS320C54XX processor. **(08 Marks)**

b. Explain the operation of serial I/O ports and hardware timer of TMS320C54XX on chip peripherals. **(08 Marks)**

c. Describe the operations of the following instructions with respect to C54XX processor.
i) MAS *AR3–, *AR4+, B, A ii) MPY #01234, A **(04 Marks)**

PART – B

5 a. What do you mean by Q notation used in DSP algorithm implementation? What are the values represented by 16 bit number N = 4000 H in Q15, Q7 and Q9 notation? **(08 Marks)**

b. Briefly explain IIR filters. **(04 Marks)**

c. Write a TMS320C54XX program that illustrates the implementation of an interpolating FIR filter of length 15 and interpolating factor 5. **(08 Marks)**

6 a. Write a TMS320C54XX program that illustrates the implementation of 8 point DIT FFT algorithm. **(12 Marks)**

b. Briefly explain scaling and derive the expression for optimum scaling factor for DIT FFT Butterfly algorithm. **(08 Marks)**

7 a. With a neat schematic diagram, design a data memory system with address range 000800h – 000FFFh for a C5416 processor. Use 2k × 8 SRAM memory chips. **(08 Marks)**

b. Explain how the interrupts are handled in TMS320C54XX processor, with the help of a flow chart. **(08 Marks)**

c. Explain briefly memory space organization in TMS320C54XX memory. **(04 Marks)**

8 Write short notes on :

a. 4 × 4 Braun multiplier b. Direct memory access

c. DSP based telemetry receiver d. Codec interface. **(20 Marks)**

* * * * *